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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/654,424	09/04/2003	Terunao Hanaoka	117031	7621

25944 7590 09/08/2004

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/654,424	HANAOKA, TERUNAO	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *18-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/11/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/654424 Attorney's Docket #: 117031
Filing Date: 9/4/2003; claimed foreign priority to 10/11/2002

Applicant: Hanaoka

Examiner: Alexander Williams

Applicant's election with traverse of species of figure 3 (claims 1-17) filed 7/9/04 is acknowledged.

Applicant's arguments have been considered are not found to be persuasive. The Examiner would be unduly burdened to evaluate all claims fully on their merit at the full time.

The requirement is still deemed proper and is therefore made FINAL.

This application contains claims 18-21 drawn to an invention non-elected with traverse. A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR § 1.144 & MPEP § 821.01).

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 to 17 are rejected under 35 U.S.C. § 102(b) as being anticipated by Fukasawa (U.S. Patent # 5,973,931).

1. Fukasawa (figures 1 to 4B) specifically figure 4A and 4B show a wiring board comprising: a substrate **11**; and an interconnect pattern which is formed on the substrate and includes a land **16**, wherein a penetration hole **(between D1 and D2, 17a)** which exposes the substrate is formed in the land, and wherein the penetration hole is formed in a region along a periphery of the land.

2. The wiring board as defined in claim 1, Fukasawa show wherein a planar shape of the land is approximately circular.

3. The wiring board as defined in claim 1, Fukasawa show wherein the penetration hole is an elongated hole.

4. The wiring board as defined in claim 3, Fukasawa show wherein the penetration hole is the elongated hole which is longer in a direction along the periphery of the land than in a direction intersecting the periphery of the land at right angles.

5. The wiring board as defined in claim 1, Fukasawa show wherein a plurality of the penetration holes are formed in the land.

6. The wiring board as defined in claim 5, Fukasawa show wherein the plurality of penetration holes are arranged in a region along the periphery of the land.

7. The wiring board as defined in claim 5, Fukasawa show wherein the plurality of penetration holes are disposed so that distance between the adjacent penetration holes is approximately the same.

8. The wiring board as defined in claim 1, Fukasawa further comprising: a resist layer **17** which is formed on a surface of the substrate on which the interconnect pattern is formed and includes an opening which exposes at least a part of the land.

9. The wiring board as defined in claim 8, Fukasawa show wherein a planar shape of the opening of the resist layer is approximately circular.

10. The wiring board as defined in claim 8, Fukasawa show wherein the resist layer covers at least a part of the penetration hole.

11. The wiring board as defined in claim 8, Fukasawa show wherein the resist layer covers the penetration hole, and wherein part of an edge of the penetration hole is in contact with an edge of the opening of the resist layer.
12. The wiring board as defined in claim 1, Fukasawa show which is formed as an interposer.
13. The wiring board as defined in claim 1, Fukasawa show which is formed as a motherboard.
14. Fukasawa show a semiconductor device comprising: the wiring board as defined in claim 1, and a semiconductor chip **2** which is electrically connected with the interconnect pattern.
15. The semiconductor device as defined in claim 14, Fukasawa further comprising an external terminal **3,13** formed on the land.
16. Fukasawa show a circuit board on which the semiconductor device as defined in claim 14 is mounted.
17. Fukasawa show an electronic equipment comprising the semiconductor device as defined in claim 14.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/780,668,696,690,691,698,700,701,774,773,680,738, 734,737,782,788 361/774,736,746,760,807,809, 174/255,356,259,260	9/6/04
Other Documentation: foreign patents and literature in 257/780,668,696,690,691,698,700,701,774,773,680, 738, 734,737,782,788 361/774,736,746,760,807,809, 174/255,356,259,260	9/6/04
Electronic data base(s): U.S. Patents EAST	9/6/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
9/7/04

Primary Patent Examiner
Alexander O. Williams